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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/055,266	01/22/2002	Ki-won Choi	9898-208	6747

20575 7590 03/27/2007
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EXAMINER

NADAV, ORI

ART UNIT	PAPER NUMBER
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2811

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/27/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/055,266

Applicant(s)

CHOI, KI-WON

Examiner

Ori Nadav

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 February 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 28-38, 40 and 42-46 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 28-38, 40 and 42-46 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 28-38, 40 and 42 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claimed limitations of "first solder ball pad, second bond finger and third bond finger", as recited in the rejected claims, are unclear as to what is the distinction between these elements and the "first printed circuit solder ball pad, second printed circuit bond finger and third printed circuit bond finger".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 28-34, 36-38, 40 and 42, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Parker et al. (5,633,785) in view of Smith (6,707,149).

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Regarding claims 28 and 43, Parker et al. teach in figure 1 and related text a semiconductor package comprising:

- a substrate 107 (see figure 3) having a plurality of first printed circuit bond fingers 106 formed on the surface of the substrate;

- a semiconductor chip 122 having a plurality of bond pads 104 formed thereon;

- a plurality of first printed circuit solder ball pads 110 formed on the surface of the substrate;

- a first printed circuit pattern 108 formed on the surface of the substrate and electrically connecting each of a group of first printed circuit bond fingers and a corresponding first solder ball pad;

- a wire bond 102 electrically connecting formed between each of the group of first printed circuit bond fingers 106 and a corresponding bond pad 104 thereby electrically connecting each of the corresponding bond pads to a first solder ball pad;

- a second printed circuit bond finger 106 formed on the surface of the substrate;

- a second printed circuit solder ball pad formed on the surface of the substrate;

- a second printed circuit pattern 108 formed on the surface of the substrate and electrically connecting the second printed circuit bond finger and the second printed circuit solder ball pads;

- a third printed circuit bond finger formed on the surface of the substrate;

- a first wire bond 102 having one end affixed to the third bond finger 106 and the other end affixed to one of the bond pads 104; and

Parker et al. do not teach a second wire bond having one end affixed to the second bond finger and the other end affixed to the third bond fingers thereby electrically connecting said one bond pad to said second printed circuit solder ball pad.

Smith teaches in figure 5B and related text a second wire bond having one end affixed to the second bond finger and the other end affixed to the third bond fingers (the horizontal line) thereby electrically connecting said one bond pad to said second printed circuit solder ball pad.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to connect a second wire bond between the second bond finger and the third bond fingers in Parker et al.'s device in order to use the device in an application which requires electrical connection between two specific pads.

Regarding claims 29-31, Parker et al. do not teach no printed circuit pattern directly connected to the third bond finger, and no wire bonding having one end directly connected to the second bond finger and the other end directly connected to any of the bond pads.

Smith teaches in figure 5B and related text no printed circuit pattern directly connected to the third bond finger, and no wire bonding having one end directly connected to the second bond finger and the other end directly connected to any of the bond pads.

It would have been obvious to one having ordinary skill in the art at the time the invention was made not to connect a printed circuit pattern directly connected to the third bond finger, and not to connect a wire bonding between the second bond finger

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and any of the bond pads, in Parker et al.'s device in order to use the device in an application which requires specific electrical connections between the pads.

Regarding claim 32, Parker et al. teach in figure 3 and related text an encapsulant 126 for encapsulating the semiconductor chip and wire bond.

Regarding claim 33, Parker et al. teach in figure 3 and related text a solder ball 127 connected to the one solder ball pad.

Regarding claim 34, Parker et al. teach in figure 3 and related text a substrate 107 is a single layer substrate on which a printed circuit pattern is formed.

Regarding claim 36, Parker et al. teach in figure 1 and related text a solder mask is not formed on the added bond finger.

Regarding claim 37, Parker et al. teach in figure 1 and related text the wire bonds are formed over the substrate.

Regarding claim 38, Parker et al. teach in figure 3 and related text a the second wire bond between the second and third bond fingers is formed on an outer region of the substrate on which the semiconductor chip is mounted.

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Regarding claim 40, Parker et al. teach in figure 3 and related text the semiconductor chip 122 is attached to the substrate 107 using an adhesive 124.

Regarding claim 42, Parker et al. teach in figure 1 and related text the first printed circuit bond fingers have the same pad shape as that of the second bond finger.

Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable Parker et al. and Smith, as applied to claim 28 above, and further in view of Sota et al. (6,064,111). Parker et al. and Smith teach substantially the entire claimed structure, as applied to claim 28 above, except a substrate is a double layer substrate.

Sota et al. teach the double layer substrate (column 7, lines 17-20).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Sota et al. into the device taught by Parker et al. and Smith in order to improve the interchangeability of the semiconductor device in the double layer substrate.

Response to Arguments

Applicant's arguments with respect to claims 28-38, 40 and 42 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Reference B is cited as being related to the claimed invention.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



O.N.
3/20/07

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PRIMARY EXAMINER
TECHNOLOGY CENTER 2800